

Aryan Sahu

MSc Microelectronics Systems Design, University of Southampton
BTech Electronics & Instrumentation, VIT Vellore

aryan_sahu@outlook.com
calceit.com
linkedin.com/in/aryan-s4hu

PROFILE

Graduate hardware engineer with a strong foundation in RTL design, full custom ASIC flows, physical design, and verification. Experienced across the complete ASIC implementation stack — from transistor-level cell design and place-and-route through to simulation-based verification and hardware-focused software tooling. Particular interests in computer architecture, SoC design, and the intersection of software engineering and hardware development. Seeking graduate roles in hardware, verification, or physical design engineering.

EDUCATION

- **University of Southampton** 2025 – 2026
MSc Microelectronics Systems Design · Ongoing Southampton, UK
 - **Modules:** VLSI Systems Design, Digital Systems Synthesis, Digital IC & Systems Design, Secure Hardware & Embedded Devices, Embedded Processors, VLSI Design Project
- **Vellore Institute of Technology** 2021 – 2025
BTech Electronics & Instrumentation Engineering · 8.15 / 10 CGPA Vellore, India
 - **Relevant modules:** VLSI Design, Digital Electronics, Embedded Systems Design, Microprocessors & Microcontrollers

PROJECTS

- **Weather Station ASIC - Full Custom Design Flow** Feb 2026 – Apr 2026
Tools: Synopsys DC, Cadence Xcelium, Encounter, Virtuoso; SystemVerilog calceit.com/projects
 - Working in a team, led overall system architecture for a weather station ASIC targeting AMS 0.35 μm , integrating SPI sensor interfaces, LCD controller, SRAM-backed memory controller, and a 48×84 pixel display.
 - Personally designed the memory controller (round-robin arbitration between rain, wind, and display modules) and the LCD controller (multi-mode display: rain, wind speed/direction, RTC, elapsed time, calibration).
 - Led synthesis using Synopsys Design Compiler, including DFT scan chain insertion, and place-and-route using Cadence Encounter; contributed to post-layout sign-off in Cadence Virtuoso.
 - Full ASIC flow: SystemVerilog RTL \rightarrow Cadence Xcelium simulation \rightarrow Synopsys DC synthesis \rightarrow Encounter P&R \rightarrow Virtuoso post-layout sign-off.
- **Custom Cell Library & Bitslice Multiplier** Dec 2025 – Jan 2026
Tools: Magic VLSI, SPICE, HSPICE, Cadence Xcelium; SystemVerilog, Python github.com/calceit/Custom-Cell-Library
 - Contributed to a 16-cell standard cell library targeting TSMC 180 nm in Magic VLSI; personally designed NAND gate and RD-type scan flip-flop cells at transistor level, verified with SPICE simulation.
 - Built a Python automation framework to parse .mag/.ext files, run HSPICE characterisation simulations, and generate a formatted cell library databook covering timing and functional behaviour.
 - Designed an 8-bit shift-and-add multiplier on the custom library, from transistor-level schematic and layout through RTL and synthesis; integrated a full scan chain (SDI/SDO/Test) with an 11-state control FSM for DFT.
 - Validated correctness across abstraction levels from individual cells through full system integration using Cadence Xcelium.
- **NEO Hardware Accelerator - Pipelined FPGA Design** November 2025
Tools: Cadence Xcelium; Intel Quartus Prime, SystemVerilog, MATLAB github.com/calceit/NEO
 - Designed a 4-stage pipelined hardware accelerator for the Nonlinear Energy Operator ($\psi[n] = x[n-1]^2 - x[n] \cdot x[n-2]$), used in biomedical signal processing for real-time neural spike detection.
 - Achieved one-sample-per-cycle throughput at full pipeline fill with a clean, hazard-free pipeline structure in SystemVerilog.
 - Generated MATLAB test vectors in 4-bit signed fixed-point arithmetic; verified RTL output against golden reference model via Cadence Xcelium simulation and Quartus Prime on Cyclone IV E FPGA.
- **Mini-AES - C++ Cryptographic Implementation** November 2025
Tools: C++17 github.com/calceit/MiniAES
 - Implemented Mini-AES in C++17, operating on 16-bit blocks with 16-bit keys; internal state represented as four 4-bit nibbles.
 - Encryption path applies initial key addition followed by two rounds of NibbleSub (4-bit S-box lookup), ShiftRow (nibble swap), MixColumns (2×2 matrix multiplication over $\text{GF}(2^4)$ modulo $x^4 + x + 1$), and round key addition.
 - Decryption path reverses the encryption sequence using an inverse S-box and inverse MixColumns.
 - Key schedule derives three 16-bit round keys (K0–K2) from the master key via nibble-level expansion with S-box substitution and RCON injection.

WORK EXPERIENCE

- **Maven Silicon** *August – October 2023*
Bangalore, India
VLSI Design Intern
 - Designed and verified a 5-stage pipelined 32-bit RISC-V processor in Verilog, implementing fetch, decode, execute, memory, and writeback stages with hazard detection and data forwarding logic.
 - Completed structured training in VLSI design methodologies covering RTL design, logic synthesis, and physical design flows.
 - Gained hands-on experience with industry-standard EDA tools and design practices in a professional environment.

TECHNICAL SKILLS

- **HDL / RTL:** SystemVerilog, Verilog
- **Physical Design:** Place-and-route (Cadence Encounter), synthesis (Synopsys DC), DFT scan insertion, floorplanning, transistor-level cell design (Magic VLSI)
- **Simulation & Verification:** Cadence Xcelium, SPICE, HSPICE, directed testbench methodology, waveform analysis, functional simulation
- **EDA Tools:** Synopsys DC, Cadence Encounter, Virtuoso, Xcelium; Magic VLSI, Quartus Prime, Xilinx Vivado, ModelSim
- **Scripting & Languages:** Python, TCL, C++17, C, MATLAB, L^AT_EX
- **Protocols & Architectures:** AXI-Lite, SPI, RISC-V ISA
- **Other:** Linux/Unix shell, Git, KiCAD

EXTRACURRICULARS & INTERESTS

- **Guitar:** Grade 8, London College of Music.
- **Toastmasters:** Vice President of Education, BRISA VIT (2024); Phoenix Award recipient.
- **Interests:** Motorsport & Cars, Competitive Squash, Computer Architecture.